

*255 N.M.T.*

*AN*

- 1 28. (New) The method of claim 27, wherein the source and
- 2 drain regions are silicided to relieve any effect of germanium in the source and
- 3 drain regions.

### REMARKS

Applicant respectfully requests reconsideration of the present application in view of the foregoing amendments and in view of the reasons which follow.

Claims 25 and 26 have been cancelled without prejudice. Claims 27 and 28 have been added. No new matter is added. No claims have been amended. Claims 1-24 and 27-28 remain pending in the application.

In paragraphs 1-5 of the Office Action, the Examiner has restricted the application to one of two inventions: Group I (claims 1-24 drawn to a method) and Group II (claims 25 and 26 drawn to a semiconductor device). Applicant respectfully traverses the restriction requirement. However, to advance prosecution, Applicant hereby affirms the election of Group I. Applicant notes that new claims 27-28 are drawn to the method of Group I.

In paragraph 6 of the Office Action, the Examiner has objected to the specification. Applicant has amended the specification in accordance with the Examiner's suggestion. No new matter is added in the amendment to the specification.

In paragraphs 7 and 8 of the Office Action, claims 1-6, 8, 12-16, 18 and 19 are rejected under 35 U.S.C. § 102 (e) as being anticipated by U.S. Patent No. 6,232,622 (Hamada).

Hamada discloses a method of manufacturing an integrated circuit including a transistor with silicon germanium channel region, the method comprising steps of; depositing an amorphous silicon germanium material above a top surface of a semiconductor substrate; annealing the amorphous silicon germanium material to form a single crystalline semiconductor layer (see column 12, lines 14-59); depositing an amorphous silicon material above the silicon germanium material; annealing the amorphous silicon material to form a single crystalline layer (see column 8, lines 3-45); the annealing temperature for the

first and second annealing steps is at or above 1100 C and below 1400 C (see column 4, lines 5-19); and providing a source region and a drain region for the transistor, the source region and the drain region being deeper than a combined thickness of the silicon germanium material and the silicon material and a channel region between the source region and the drain region includes a thin semiconductor germanium region (see figure 8). After forming the amorphous silicon material and before providing a source and drain region a gate structure is provided (see figure 11), this will inherently form source and drain extensions. Hamada also discloses an annealing step taking place at a temperature sufficient to melt the amorphous semiconductor layer and is below the melting temperature of the substrate (see column 4, lines 5-19). The annealing steps are performed by an excimer laser using a wavelength of 308 nanometers (see column 6, lines 53-65). An oxide layer 6 is provided after the second annealing step.

Applicant respectfully traverses the rejection.

Each of independent claims 1, 12, 19 and 27 recites that amorphous semiconductor material is provided above a semiconductor substrate and that the semiconductor substrate is used to provide the source region and the drain region. For example, claim 1 recites:

providing an amorphous semiconductor material above a bulk substrate of semiconductor material . . .

doping the . . . substrate . . . to form a source region and a drain region

In another example, Claim 12 recites:

a top surface of a semiconductor substrate . . .

providing a source region and a drain region for the transistor the source region and the drain region extending into the substrate.

In a further example, Claim 19 recites:

a top surface of a semiconductor substrate . . .

providing a source region and a drain region for the transistor the source region and the drain region extended into the substrate.

In yet another example Claim 27 recites:

providing an amorphous semiconductor material above a bulk substrate of semiconductor material . . .

doping the . . . substrate. . . to form a source region and a drain region.

Thus, each independent claim specifically recites an amorphous layering process which uses a semiconductor substrate to form the source and drain regions.

Applicant notes that this process is related to the process claimed in application number 09/599,270. Claims 12-20 in application serial No. 091599,270 are indicated as allowable and a Notice of Allowance is expected shortly. The most recent Office Action for the related application is attached hereto for the Examiner's convenience.

Applicant notes that significant advantages are achieved by using the substrate for formation of the drain region as well as the transformed amorphous regions. The present application states:

Channel region 31 including layers 43 and 45 is preferably almost as deep as extensions 23 and 25. Channel region 41 is significantly shallower than the deep regions (contact locations) associated with source region 22 and drain region 24. Accordingly, sufficient depth is available for making contact to source region 22 and drain region 24 and yet a thin channel region 41 including silicon germanium layer 45 is attained. The use of layer 45 including germanium allows the mobility of carriers to be approximately 2-5 times larger than a channel region 41 comprised solely of silicon material.

The interface between layer 45 and substrate 14 is preferably extremely sharp in the vertical direction. An ideal design has a very clearly defined

Present application page 6, line 27 – page 7, line 6. Therefore, the process of independent claims 1, 13, 19 and 27 includes process steps which provide significant advantages over conventional processes.

In contrast, Hamada is not even related to the art associated with transistors formed on semiconductor substrates. In fact, Hamada is related to a thin film transistor (TFT) technology which does not utilize a semiconductor substrate. Accordingly, Hamada is missing two limitations in independent claims 1, 12, 19 and 27: 1. a semiconductor substrate is missing; and 2. a step of using the semiconductor substrate to form source and drain regions is missing.

First, Hamada only discloses one type of substrate (identified as substrate 1 throughout the Figures). Substrate 1 in Hamada is a transparent insulating substrate 1 made of glass or quartz by means of LPCVD. See Hamada, col. 3, lines 34-39. Nowhere is a semiconductor substrate shown, described or suggested. More particularly, the substrate of the TFT makes it particularly ill-suited for the solution of the present invention.

Second, claims 1, 12, 19 and 27 explicitly recite a step of forming source and drain regions utilizing the substrate. However, substrate 1 of Hamada is not utilized in the formation of the source and drain regions. Poly-crystallization silicon layer 3 is utilized for forming source and drain regions. Source and drain regions do not extend into the substrate 1 of Hamada. Indeed, it would be impracticable to form source and drain regions in substrate 1 because substrate 1 of Hamada is glass or quartz. See Hamada, col. 5 lines 12-17.

Accordingly, Hamada does not teach each and every limitation of independent claims 1, 12, 19 and 27. Therefore, withdrawal of the rejection of claims 1-6, 8, 12-16, 18 and 19 under 35 U.S.C. § 102(e) is respectfully requested.

In paragraphs 9 and 10 of the Office Action, claims 7, 9-11, 17 and 10-24 are rejected under 35 U.S.C. § 103 as being unpatentable over Hamada in view of U.S. Patent No. 5,683,934 (Candelaria). The Examiner states:

Hamada is applied as above but lacks anticipation on disclosing a semiconductor substrate including single crystalline silicon; disclosing a thickness of 100-150 angstroms for the silicon material; and disclosing a thickness of 200-500 angstroms for the silicon germanium material.

Candelaria discloses a method for making an enhanced mobility semiconductor device comprising a channel layer 12 with a thickness of 200-500 angstroms and an epitaxial layer 13 with a thickness of 100-150 angstroms (see column 3, lines 50-57). In view of this disclosure it would have been obvious to a person having ordinary skills in the art at the time the invention was made to disclose a thickness of 100-150 angstroms for a silicon material, and to disclose a thickness of 200-500 angstroms for a silicon germanium material as disclosed in Candelaria in the primary reference to Hamada because these are conventional thickness values used to fabricate channel regions. Furthermore the thickness values are only considered to be the "optimum" thickness values of the values disclosed by the Prior Art that a person having ordinary skill in the art would have been able to determine using routine experimentation based, among other things, on the desired accuracy, manufacturing costs, etc. (see In re Boesch, 205 USPQ 215 (CCPA 1980)).

Applicant respectfully traverses the rejection. Hamada and Candelaria are referred to below as the cited art.

Hamada and Candelaria cannot be properly combined to teach the process recited in claims 1-24 and 27-28. Candelaria is related to a bulk substrate technology. As discussed above, this technology is not related to the TFT technology employed in Hamada. TFT transistor technology is not at all related to the problem solved by the present invention as evidenced by the discussions of semiconductor substrates above. Accordingly, one of ordinary skill in the art forming transistors in bulk substrates would not consider the TFT technology of Hamada.

Further, there is no suggestion to substitute the amorphous layers of Hamada into Candelaria. In fact, Candelaria explicitly teaches the use of epitaxial layers formed by MOCVD molecular beam epitaxy, or ultra-high vacuum chemical vapor deposition. As discussed in the Background of the Invention of the present application, such

techniques are inefficient and are not commercially feasible for forming for single crystalline layers. See present application page 2, line 26 – page 3, line 4. Thus, one of ordinary skill in the art would be more likely to ignore Candelaria because it forms the channel layers by a process which is commercially impracticable.

Further, Candelaria clearly teaches against the use of silicon/germanium layers. Rather, a silicon carbon layer is suggested. Candelaria states:

This structure has several disadvantages including the migration of carriers out of the strained  $\text{Si}_{1-x}\text{Ge}_x$  channel layer into the relaxed  $\text{Si}_{1-y}\text{Ge}_y$  alloy layer thus reducing the enhanced mobility effect, greater alloy scattering effects because of the presence of germanium in the channel layer, and added process complexity because of multiple SiGe layers.

Accordingly, one of ordinary skill in the art combining Candelaria with Hamada would utilize silicon carbon layer rather than the explicitly claimed silicon germanium layer. This is especially true since Hamada merely makes a passing reference to the use of a germanium containing layer. Therefore, even if the cited art is combined, one of ordinary skill in the art would not achieve the invention defined in claims 1, 12, 19 and 27. Therefore, claims 1-24 and 26-27 are patentable over the cited art.

The fact that Candelaria teaches away from silicon germanium and is strong indicia of non-obviousness. Candelaria explicitly states that germanium is not appropriate and strongly urges the use of silicon carbon alloys. Candelaria states:

A carbon-doped silicon channel layer is preferred over a germanium-doped silicon channel layer because a carbon-doped channel layer has a lower alloy/carrier scattering effect. See Candelaria, column 3, lines 58-60.

Therefore, Candelaria cannot be properly combined with Hamada because it teaches away from the present application.

Independent claims 12, 19 and 26 and dependent claims 2, 3, 4, 5, 6 are patentable over the cited art for additional reasons. Each of these claims recites a channel region that includes a cap layer over the germanium-containing layer. None of

the cited art shows, describes or suggests such a feature. As discussed in the present application, the silicon layer advantageously protects in integrity of the dielectric layer from the effects of germanium. See present application page 6, lines 15-24.

Although Hamada appears to show a compound formation of layers in Figure 8, there is no suggestion of providing different material in each layer. Rather, layer 3 is comprised of poly-crystalline regions and mono-crystalline regions 102. There is no suggestion for providing different types of layers (e.g., germanium and non-germanium containing layers) in the channel region.

Hamada merely mentions the use of films including germanium. With respect to Figure 10 of Hamada, it is noted that the entire poly-silicon layer 2 is discussed as being replaced by an entirely germanium containing layer. See Hamada, column 8, lines 15-45 and column 12, lines 13-37. Further, there is no recognition of the use of the cap layer to protect the dielectric layer from germanium.

As discussed above, Candelaria does not even teach the use of silicon and germanium, much less the use of a silicon cap layer to protect the dielectric layer from germanium. Therefore, it is respectfully submitted that claims 12 and its dependent claims 13-18, claim 19 and its dependent claims 20-24, claim 27 and its dependent claim 20, and dependent claims 2-6 are patentable over the cited art.

Further, it is respectfully submitted that the Examiner is impermissibly picking and choosing features of the claims using hindsight as he selects the substrate 11 of Candelaria with a layer 3 of Hamada and a layer 13 of Candelaria. Layer 13 of Candelaria is modified to be formed by the process of forming layer 3 of Hamada without any teaching Candelaria or Hamada. Indeed, there is not even a teaching for the purpose of the silicon layer, the teaching to prevent the adverse affects of germanium with respect to the dielectric layer. Thus, claims 1-24 and 27-28 are patentable over the cited art.

Applicant believes that the present application is now in condition for allowance. Favorable reconsideration of the application as amended is respectfully requested.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

Respectfully submitted,

Date 12-6-01

FOLEY & LARDNER  
Firstar Center  
777 East Wisconsin Avenue  
Milwaukee, Wisconsin 53202-5367  
Telephone: (414) 297-5768  
Facsimile: (414) 297-4900

By Joseph N. Ziebert

Joseph N. Ziebert  
Attorney for Applicant  
Registration No. 35,421

**VERSION WITH MARKINGS TO SHOW CHANGES MADE**

The present application entitled, "A Process For Manufacturing Transistors Having Silicon/Germanium Channel Regions," is related to U.S. Application Serial No. 09/599,270 [ \_\_\_\_\_ ], filed on an even date herewith by Yu (Attorney Docket No. 39153-268).